Behzad Razavi

DESIGN OF Analog CMOS Integrated Circuits

Mc Graw Hill Education

SECOND EDITION

Design of Analog CMOS Integrated Circuits

Second Edition

Behzad Razavi

Professor of Electrical Engineering
University of California, Los Angeles

Mc Graw Hill Education

DESIGN OF ANALOG CMOS INTEGRATED CIRCUITS, SECOND EDITION

1 2 3 4 5 6 7 8 9 0 QVS/QVS 1 0 9 8 7 6

ISBN 978-0-07-252493-2
MHID 0-07-252493-6

Senior Vice President, Products & Markets: *Kurt L. Strand*
Vice President, General Manager, Products & Markets: *Marty Lange*
Vice President, Content Design & Delivery: *Kimberly Meriwether David*
Managing Director: *Thomas Timp*
Global Brand Manager: *Raghu Srinivasan*
Director, Product Development: *Rose Koos*
Product Developer: *Vincent Bradshaw*
Marketing Manager: *Nick McFadden*
Director of Digital Content: *Chelsea Haupt, Ph. D*
Director, Content Design & Delivery: *Linda Avenarius*
Program Manager: *Faye M. Herrig*
Content Project Managers: *Heather Ervolino; Sandra Schnee*
Buyer: *Jennifer Pickel*
Content Licensing Specialists: *Lorraine Buczek* (*Text*)
Compositor: *MPS Limited*
Printer: *Quad/Graphics*

Library of Congress Cataloging-in-Publication Data

Razavi, Behzad.
Design of analog CMOS integrated circuits / Behzad Razavi, professor of electrical engineering, University of California, Los Angeles. – Second edition.
pages cm
Includes bibliographical references and index.
ISBN 978-0-07-252493-2 (alk. paper) – ISBN 0-07-252493-6 (alk. paper) 1. Analog CMOS integrated circuits. 2. Linear integrated circuits–Design and construction. 3. Metal oxide semiconductors, Complementary. I. Title.
TK7874.654.R39 2017
621.3815–dc23 2015035303

mheducation.com/highered

To the memory of my parents

Preface to the Second Edition

When I submitted proposals to publishers for the first edition of this book, they posed two questions to me: (1) What is the future demand for analog books in a digital world? and (2) Is it wise to publish a book dealing solely with CMOS? The words "analog" and "CMOS" in the book's title were both in question.

Fortunately, the book resonated with students, instructors, and engineers. It has been adopted by hundreds of universities around the world, translated to five languages, and cited 6,500 times.

While many fundamentals of analog design have not changed since the first edition was introduced, several factors have called for a second: migration of CMOS technologies to finer geometries and lower supply voltages, new approaches to analysis and design, and the need for more detailed treatments of some topics. This edition provides:

- Greater emphasis on modern CMOS technology, culminating in a new chapter, Chapter 11, on design methodologies and step-by-step op amp design in nanometer processes
- Extensive study of feedback through the approaches by Bode and Middlebrook
- A new section on the analysis of stability using Nyquist's approach—as the oft-used Bode method falls short in some common systems
- Study of FinFETs
- Sidebars highlighting important points in nanometer design
- A new section on biasing techniques
- Study of low-voltage bandgap circuits
- More than 100 new examples

Some instructors ask why we begin with square-law devices. This is for two reasons: (1) such a path serves as an intuitive entry point and provides considerable value in the analysis of amplifiers in terms of allowable voltage swings, and (2) despite their very short channel lengths, FinFETs—the devices used in 16-nm nodes and below—exhibit nearly square-law characteristics.

This book is accompanied with a solutions manual and a new set of PowerPoint slides, available at www.mhhe.com/razavi.

Behzad Razavi
July 2015

Preface to the First Edition

In the past two decades, CMOS technology has rapidly embraced the field of analog integrated circuits, providing low-cost, high-performance solutions and rising to dominate the market. While silicon bipolar and III-V devices still find niche applications, only CMOS processes have emerged as a viable choice for the integration of today's complex mixed-signal systems. With channel lengths projected to scale down to 0.05 μm, CMOS technology will continue to serve circuit design for another two decades.

Analog circuit design itself has evolved with the technology as well. High-voltage, high-power analog circuits containing a few tens of transistors and processing small, continuous-time signals have gradually been replaced by low-voltage, low-power systems comprising thousands of devices and processing large, mostly discrete-time signals. For example, many analog techniques used only ten years ago have been abandoned because they do not lend themselves to low-voltage operation.

This book deals with the analysis and design of analog CMOS integrated circuits, emphasizing fundamentals as well as new paradigms that students and practicing engineers need to master in today's industry. Since analog design requires both intuition and rigor, each concept is first introduced from an intuitive perspective and subsequently treated by careful analysis. The objective is to develop both a solid foundation and methods of analyzing circuits by inspection so that the reader learns what approximations can be made in which circuits and how much error to expect in each approximation. This approach also enables the reader to apply the concepts to bipolar circuits with little additional effort.

I have taught most of the material in this book both at UCLA and in industry, polishing the order, the format, and the content with every offering. As the reader will see throughout the book, I follow four "golden rules" in writing (and teaching): (1) I explain *why* the reader needs to know the concept that is to be studied; (2) I put myself in the reader's position and predict the questions that he/she may have while reading the material for the first time; (3) With Rule 2 in mind, I pretend to know only as much as the (first-time) reader and try to "grow" with him/her, thereby experiencing the same thought process; (4) I begin with the "core" concept in a simple (even imprecise) language and gradually add necessary modifications to arrive at the final (precise) idea. The last rule is particularly important in teaching circuits because it allows the reader to observe the evolution of a topology and hence learn both analysis and synthesis.

The text comprises 16 chapters whose contents and order are carefully chosen to provide a natural flow for both self-study and classroom adoption in quarter or semester systems. Unlike some other books on analog design, we cover only a *bare minimum* of MOS device physics at the beginning, leaving more advanced properties and fabrication details for later chapters. To an expert, the elementary device physics treatment my appear oversimplified, but my experience suggests that (a) first-time readers simply do not absorb the high-order device effects and fabrication technology before they study circuits because they do not see the relevance; (b) if properly presented, even the simple treatment proves adequate for a substantial coverage of basic circuits; (c) readers learn advanced device phenomena and processing steps much more readily *after* they have been exposed to a significant amount of circuit analysis and design.

Chapter 1 provides the reader with motivation for learning the material in this book. Chapter 2 describes basic physics and operation of MOS devices.

Chapters 3 through 5 deal with single-stage and differential amplifiers and current mirrors, respectively, developing efficient analytical tools for quantifying the behavior of basic circuits by inspection.

Chapters 6 and 7 introduce two imperfections of circuits, namely, frequency response and noise. Noise is treated at an early stage so that it "sinks in" as the reader accounts for its effects in subsequent circuit developments.

Chapters 8 through 10 describe feedback, operational amplifiers, and stability in feedback systems, respectively. With the useful properties of feedback analyzed, the reader is motivated to design high-performance, stable op amps and understand the trade-offs between speed, precision, and power dissipation.

Chapters 11 through 13 deal with more advanced topics: bandgap references, elementary switched-capacitor circuits, and the effect of nonlinearity and mismatch. These three subjects are included here because they prove essential in most analog and mixed-signal systems today.

Chapter 14 is concerned with high-order MOS device effects and models, emphasizing the circuit design implications. If preferred, the chapter can directly follow Chapter 2 as well. Chapter 15 describes CMOS fabrication technology with a brief overview of layout design rules.

Chapter 16 presents the layout and packaging of analog and mixed-signal circuits. Many practical issues that directly impact the performance of the circuit are described and various techniques are introduced.

The reader is assumed to have a basic knowledge of electronic circuits and devices, e.g., *pn* junctions, the concept of small-signal operation, equivalent circuits, and simple biasing. For a senior-level elective course, Chapters 1 through 8 can be covered in a quarter and Chapters 1 through 10 in a semester. For a first-year graduate course, Chapters 1 through 11 plus one of Chapters 12, 13, or 14 can be taught in one quarter, and almost the entire book in one semester.

The problem sets at the end of each chapter are designed to extend the reader's understanding of the material and complement it with additional practical considerations. A solutions manual will be available for instructors.

Behzad Razavi
July 2000

Acknowledgments for the Second Edition

The second edition was enthusiastically and meticulously reviewed by a large number of individuals in academia and industry. It is my pleasure to acknowldege their contributions:

Saheed Adeolu Tijani (University of Pavia)
Firooz Aflatouni (University of Pennsylvania)
Pietro Andreani (Lund University)
Emily Allstot (University of Washington)
Tejasvi Anand (University of Illinois, Urbana-Champaign)
Afshin Babveyh (Stanford)
Nima Baniasadi (UC Berkeley)
Sun Yong Cho (Seoul National University)
Min Sung Chu (Seoul National University)
Yi-Ying Cheng (UCLA)
Jeny Chu (UCLA)
Milad Darvishi (Qualcomm)
Luis Fei (Intel)
Andrea Ghilioni (University of Pavia)
Chengkai Gu (UCLA)
Payam Heydari (UC Irvine)
Cheng-En Hsieh (National Taiwan University)
Po-Chiun Huang (National Tsing-Hua University)
Deog-Kyoon Jeong (Seoul National University)
Nader Kalantari (Broadcom)

Alireza Karimi (UC Irvine)
Ehsan Kargaran (University of Pavia)
Sotirios Limotyrakis (Qualcomm Atheros)
Xiaodong Liu (Lund University)
Nima Maghari (University of Florida)
Shahriar Mirabbasi (University of British Columbia)
Hossein Mohammadnezhad (UC Irvine)
Amir Nikpaik (University of British Columbia)
Aria Samiei (University of Southern California)
Kia Salimi (IMEC)
Alireza Sharif-Bakhtiar (University of Toronto)
Guanghua Shu (University of Illinois, Urbana-Champaign)
David Su (Qualcomm Atheros)
Siyu Tan (Lund University)
Jeffrey Wang (University of Toronto)
Tzu-Chao Yan (National Chiao-Tung University)
Ehzan Zhian Tabasy (University of Texas A&M)

In addition, my colleague Jason Woo explained to me many subtleties of nanometer devices and their physics. I wish to thank all.

The production of the book has been in the hands of Heather Ervolino and Vincent Bradshaw of McGraw-Hill, who tirelessly attended to every detail over a six-month period. I would like to thank both.

Finally, I wish to thank my wife, Angelina, for her continual help with typing and organizing the chapters.

Acknowledgments for the First Edition

Writing a book begins with a great deal of excitement. However, after two years of relentless writing, drawing, and revising, when the book exceeds 700 pages and it is almost impossible to make the equations and subscripts and superscripts in the last chapter consisent with those in the first, the author begins to feel streaks of insanity, realizing that the book will never finish without the support of many other people.

This book has benefited from the contributions of many individuals. A number of UCLA students read the first draft and the preview edition sentence by sentence. In particular, Alireza Zolfaghari, Ellie Cijvat, and Hamid Rafati meticulously read the book and found several hundred errors (some quite subtle). Also, Emad Hegazi, Dawei Guo, Alireza Razzaghi, Jafar Savoj, and Jing Tian made helpful suggestions regarding many chapters. I thank all.

Many experts in academia and industry read various parts of the book and provided useful feedback. Among them are Brian Brandt (National Semiconductor), Matt Corey (National Semiconductor), Terri Fiez (Oregon State University), Ian Galton (UC San Diego), Ali Hajimiri (Caltech), Stacy Ho (Analog Devices), Yin Hu (Texas Instruments), Shen-Iuan Liu (National Taiwan University), Joe Lutsky (National Semiconductor), Amit Mehrotra (University of Illinois, Urbana-Champaign), David Robertson (Analog Devices), David Su (T-Span), Tao Sun (National Semiconductor), Robert Taft (National Semiconductor), and Masoud Zargari (T-Span). Jason Woo (UCLA) patiently endured and answered my questions about device physics. I thank all.

Ramesh Harjani (University of Minnesota), John Nyenhius (Purdue University), Norman Tien (Cornell University), and Mahmoud Wagdy (California State University, Long Beach) reviewed the book proposal and made valuable sugegstions. I thank all.

My wife, Angelina, has made many contributions to this book, from typing chapters to finding numerous errors and raising questions that made me reexamine my own understanding. I am very grateful to her.

The timely production of the book was made possible by the hard work of the staff at McGraw-Hill, particularly Catherine Fields, Michelle Flomenhoft, Heather Burbridge, Denise Santor-Mitzit, and Jim Labeots. I thank all.

I learned analog design from two masters: Mehrdad Sharif-Bakhtiar (Sharif University of Technology) and Bruce Wooley (Stanford University), and it is only appropriate that I express my gratitude to them here. What I inherited from them will be inherited by many generations of students.

About the Author

Behzad Razavi received the BSEE degree from Sharif University of Technology in 1985 and the MSEE and PhDEE degrees from Stanford University in 1988 and 1992, respectively. He was with AT&T Bell Laboratories and Hewlett-Packard Laboratories until 1996. Since 1996, he has been Associate Professor and subsequently Professor of Electrical Engineering at University of California, Los Angeles. His current research includes wireless transceivers, frequency synthesizers, phase-locking and clock recovery for high-speed data communications, and data converters.

Professor Razavi was an Adjunct Professor at Princeton University from 1992 to 1994, and at Stanford University in 1995. He served on the Technical Program Committees of the International Solid-State Circuits Conference (ISSCC) from 1993 to 2002 and VLSI Circuits Symposium from 1998 to 2002. He has also served as Guest Editor and Associate Editor of the *IEEE Journal of Solid-State Circuits*, *IEEE Transactions on Circuits and Systems*, and *International Journal of High Speed Electronics*.

Professor Razavi received the Beatrice Winner Award for Editorial Excellence at the 1994 ISSCC, the best paper award at the 1994 European Solid-State Circuits Conference, the best panel award at the 1995 and 1997 ISSCC, the TRW Innovative Teaching Award in 1997, the best paper award at the IEEE Custom Integrated Circuits Conference in 1998, and the McGraw-Hill First Edition of the Year Award in 2001. He was the corecipient of both the Jack Kilby Outstanding Student Paper Award and the Beatrice Winner Award for Editorial Excellence at the 2001 ISSCC. He received the Lockheed Martin Excellence in Teaching Award in 2006, the UCLA Faculty Senate Teaching Award in 2007, and the CICC Best Invited Paper Award in 2009 and in 2012. He was the corecipient of the 2012 VLSI Circuits Symposium Best Student Paper Award and the 2013 CICC Best Paper Award. He was also recognized as one of the top 10 authors in the 50-year history of ISSCC. He received the 2012 Donald Pederson Award in Solid-State Circuits and the American Society for Engineering Education PSW Teaching Award in 2014.

Professor Razavi has served as an IEEE Distinguished Lecturer and is a Fellow of IEEE. He is the author of *Principles of Data Conversion System Design*, *RF Microelectronics*, *Design of Analog CMOS Integrated Circuits*, *Design of Integrated Circuits for Optical Communications*, and *Fundamentals of Microelectronics,* and the editor of *Monolithic Phase-Locked Loops and Clock Recovery Circuits* and *Phase-Locking in High-Performance Systems.*

Brief Contents

Contents

CHAPTER

1

Introduction to Analog Design

1.1 ■ Why Analog?

We are surrounded by "digital" devices: digital cameras, digital TVs, digital communications (cell phones and WiFi), the Internet, etc. Why, then, are we still interested in analog circuits? Isn't analog design old and out of fashion? Will there even be jobs for analog designers ten years from now?

Interestingly, these questions have been raised about every five years over the past 50 years, but mostly by those who either did not understand analog design or did not want to deal with its challenges. In this section, we learn that analog design is still essential, relevant, and challenging and will remain so for decades to come.

1.1.1 Sensing and Processing Signals

Many electronic systems perform two principal functions: they sense (receive) a signal and subsequently process and extract information from it. Your cell phone receives a radio-frequency (RF) signal and, after processing it, provides voice or data information. Similarly, your digital camera senses the light intensity emitted from various parts of an object and processes the result to extract an image.

We know intuitively that the complex task of *processing* is preferably carried out in the digital domain. In fact, we may wonder whether we can directly digitize the signal and avoid *any* operations in the analog domain. Figure 1.1 shows an example where the RF signal received by the antenna is digitized by an analog-to-digital converter (ADC) and processed entirely in the digital domain. Would this scenario send analog and RF designers to the unemployment office?

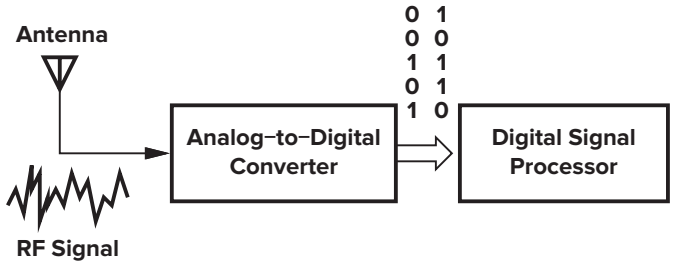


Figure 1.1 Hypothetical RF receiver with direct signal digitization.

The answer is an emphatic no. An ADC that could digitize the minuscule RF signal[1] would consume much more power than today's cell phone receivers. Furthermore, even if this approach were seriously considered, only *analog* designers would be able to develop the ADC. The key point offered by this example is that the sensing *interface* still demands high-performance analog design.

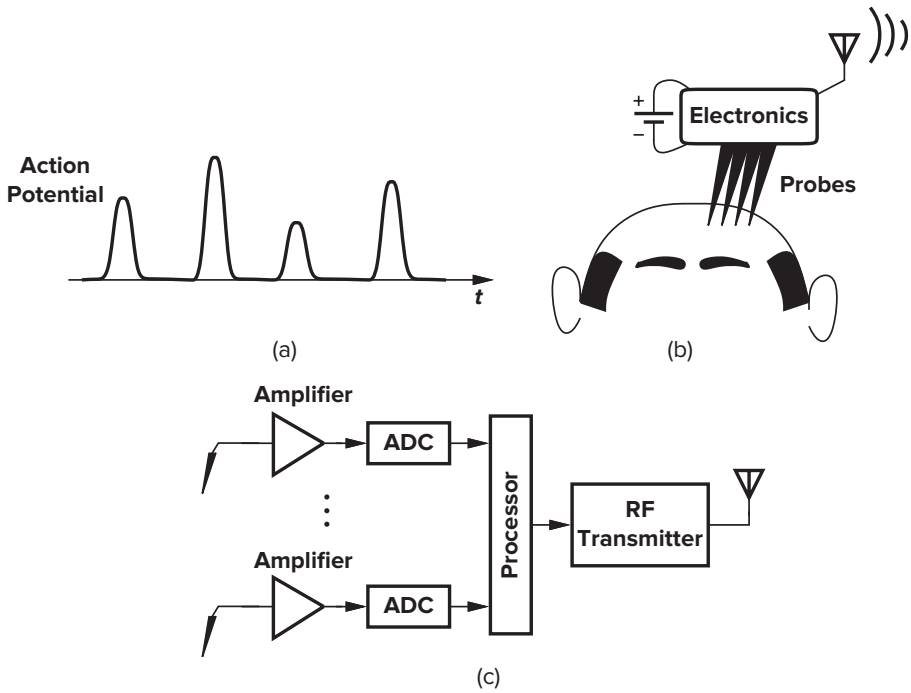


Figure 1.2 (a) Voltage waveform generated as a result of neural activity, (b) use of probes to measure action potentials, and (c) processing and transmission of signals.

Another interesting example of sensing challenges arises in the study of the brain signals. Each time a neuron in your brain "fires," it generates an electric pulse with a height of a few millivolts and a duration of a few hundred microseconds [Fig. 1.2(a)]. To monitor brain activities, a neural recording system may employ tens of "probes" (electrodes) [Fig. 1.2(b)], each sensing a series of pulses. The signal produced by each probe must now be amplified, digitized, and transmitted *wirelessly* so that the patient is free to move around [Fig. 1.2(c)]. The sensing, processing, and transmission electronics in this environment must consume a low amount of power for two reasons: (1) to permit the use of a small battery for days or weeks, and (2) to minimize the rise in the chip's temperature, which could otherwise damage the patient's tissue. Among the functions shown in Fig. 1.2(c), the amplifiers, the ADCs, and the RF transmitter—all analog circuits—consume most of the power.

1.1.2 When Digital Signals Become Analog

The use of analog circuits is not limited to analog signals. If a digital signal is so small and/or so distorted that a digital gate cannot interpret it correctly, then the analog designer must step in. For example, consider a long USB cable carrying data rate of hundreds of megabits per second between two laptops. As shown in Fig. 1.3, Laptop 1 delivers the data to the cable in the form of a sequence of ONEs and ZERO.

[1] And withstand large unwanted signals.

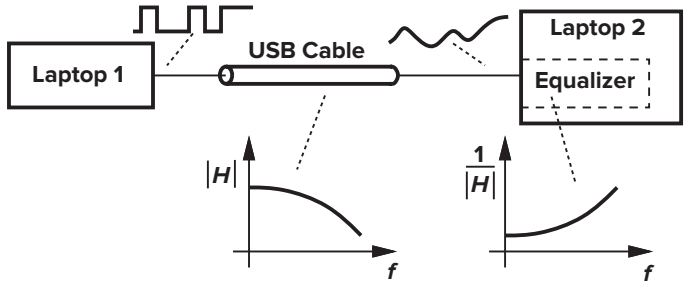


Figure 1.3 Equalization to compensate for high-frequency attenuation in a USB cable.

Unfortunately, the cable exhibits a finite bandwidth, attenuating high frequencies and distorting the data as it reaches Laptop 2. This device must now perform sensing and processing, the former requiring an analog circuit (called an "equalizer") that corrects the distortion. For example, since the cable attenuates high frequencies, we may design the equalizer to *amplify* such frequencies, as shown conceptually by the $1/|H|$ plot in Fig. 1.3.

The reader may wonder whether the task of equalization in Fig. 1.3 could be performed in the digital domain. That is, could we directly digitize the received distorted signal, digitally correct for the cable's limited bandwidth, and then carry out the standard USB signal processing? Indeed, this is possible if the ADC required here demands less power and less complexity than the analog equalizer. Following a detailed analysis, the analog designer decides which approach to adopt, but we intuitively know that at very high data rates, e.g., tens of gigabits per second, an analog equalizer proves more efficient than an ADC.

The above equalization task exemplifies a general trend in electronics: at lower speeds, it is more efficient to digitize the signal and perform the required function(s) in the digital domain, whereas at higher speeds, we implement the function(s) in the analog domain. The speed boundary between these two paradigms depends on the nature of the problem, but it has risen over time.

1.1.3 Analog Design Is in Great Demand

Despite tremendous advances in semiconductor technology, analog design continues to face new challenges, thus calling for innovations. As a gauge of the demand for analog circuits, we can consider the papers published by industry and academia at circuits conferences and see what percentage fall in our domain. Figure 1.4 plots the number of analog papers published at the International Solid-State Circuits

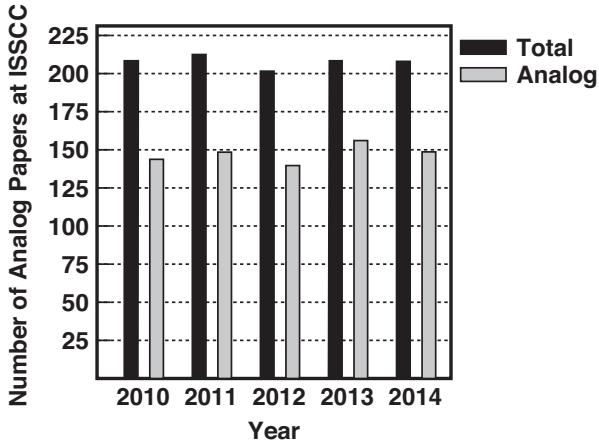


Figure 1.4 Number of analog papers published at the ISSCC in recent years.

Conference (ISSCC) in recent years, where "analog" is defined as a paper requiring the knowledge in this book. We observe that the *majority* of the papers involve analog design. This is true even though analog circuits are typically quite a lot less complex than digital circuits; an ADC contains several thousand transistors whereas a microprocessor employs billions.

1.1.4 Analog Design Challenges

Today's analog designers must deal with interesting and difficult problems. Our study of devices and circuits in this book will systematically illustrate various issues, but it is helpful to take a brief look at what lies ahead.

Transistor Imperfections As a result of scaling, MOS transistors continue to become *faster,* but at the cost of their "analog" properties. For example, the maximum voltage gain that a transistor can provide declines with each new generation of CMOS technology. Moreover, a transistor's characteristics may depend on its *surroundings*, i.e., the size, shape, and distance of other components around it on the chip.

Declining Supply Voltages As a result of device scaling, the supply voltage of CMOS circuits has inevitably fallen from about 12 V in the 1970s to about 0.9 V today. Many circuit configurations have not survived this supply reduction and have been discarded. We continue to seek new topologies that operate well at low voltages.

Power Consumption The semiconductor industry, more than ever, is striving for low-power design. This effort applies both to portable devices—so as to increase their battery lifetime—and to larger systems—so as to reduce the cost of heat removal and ease their drag on the earth's resources. MOS device scaling directly lowers the power consumption of digital circuits, but its effect on analog circuits is much more complicated.

Circuit Complexity Today's analog circuits may contain tens of thousands of transistors, demanding long and tedious simulations. Indeed, modern analog designers must be as adept at SPICE as at higher-level simulators such as MATLAB.

PVT Variations Many device and circuit parameters vary with the fabrication process, supply voltage, and ambient temperature. We denote these effects by PVT and design circuits such that their performance is acceptable for a specified range of PVT variations. For example, the supply voltage may vary from 1 V to 0.95 V and the temperature from 0° to 80°. Robust analog design in CMOS technology is a challenging task because device parameters vary significantly across PVT.

1.2 ■ Why Integrated?

The idea of placing multiple electronic devices on the same substrate was conceived in the late 1950s. In 60 years, the technology has evolved from producing simple chips containing a handful of components to fabricating flash drives with one trillion transistors as well as microprocessors comprising several billion devices. As Gordon Moore (one of the founders of Intel) predicted in the early 1970s, the number of transistors per chip has continued to double approximately every one and a half years. At the same time, the minimum dimension of transistors has dropped from about 25 μm in 1960 to about 12 nm in the year 2015, resulting in a tremendous improvement in the speed of integrated circuits.

Driven primarily by the memory and microprocessor market, integrated-circuit technologies have also embraced analog design, affording a complexity, speed, and precision that would be impossible to achieve using discrete implementations. We can no longer build a discrete prototype to predict the behavior and performance of modern analog circuits.

1.3 ■ Why CMOS?

The idea of metal-oxide-silicon field-effect transistors (MOSFETs) was patented by J. E. Lilienfeld in the early 1930s—well before the invention of the bipolar transistor. Owing to fabrication limitations, however, MOS technologies became practical only much later, in the early 1960s, with the first several generations producing only n-type transistors. It was in the mid-1960s that complementary MOS (CMOS) devices (i.e., with both n-type and p-type transistors) were introduced, initiating a revolution in the semiconductor industry.

CMOS technologies rapidly captured the digital market: CMOS gates dissipated power only during switching and required very few devices, two attributes in sharp contrast to their bipolar or GaAs counterparts. It was also soon discovered that the dimensions of MOS devices could be scaled down more easily than those of other types of transistors.

The next obvious step was to apply CMOS technology to analog design. The low cost of fabrication and the possibility of placing both analog and digital circuits on the same chip so as to improve the overall performance and/or reduce the cost of packaging made CMOS technology attractive. However, MOSFETs were slower and noisier than bipolar transistors, finding limited application.

How did CMOS technology come to dominate the analog market as well? The principal force was device scaling because it continued to improve the speed of MOSFETs. The intrinsic speed of MOS transistors has increased by orders of magnitude in the past 60 years, exceeding that of bipolar devices even though the latter have also been scaled (but not as fast).

Another critical advantage of MOS devices over bipolar transistors is that the former can operate with lower supply voltages. In today's technology, CMOS circuits run from supplies around 1 V and bipolar circuits around 2 V. The lower supplies have permitted a smaller power consumption for complex integrated circuits.

1.4 ■ Why This Book?

The design of analog circuits itself has evolved together with the technology and the performance requirements. As the device dimensions shrink, the supply voltage of intergrated circuits drops, and analog and digital circuits are fabricated on one chip, many design issues arise that were previously unimportant. Such trends demand that the analysis and design of circuits be accompanied by an in-depth understanding of new technology-imposed limitations.

Good analog design requires intuition, rigor, and creativity. As analog designers, we must wear our engineer's hat for a quick and intuitive understanding of a large circuit, our mathematician's hat for quantifying subtle, yet important effects in a circuit, and our artist's hat for inventing new circuit topologies.

This book describes modern analog design from both intuitive and rigorous angles. It also fosters the reader's creativity by carefully guiding him or her through the evolution of each circuit and presenting the thought process that occurs during the development of new circuit techniques.

1.5 ■ Levels of Abstraction

Analysis and design of integrated circuits often require thinking at various levels of abstraction. Depending on the effect or quantity of interest, we may study a complex circuit at device physics level, transistor level, architecture level, or system level. In other words, we may consider the behavior of individual devices in terms of their internal electric fields and charge transport [Fig. 1.5(a)], the interaction of a group of devices according to their electrical characteristics [Fig. 1.5(b)], the function of several building blocks operating as a unit [Fig. 1.5(c)], or the performance of the system in terms of that of its constituent subsystems

[Fig. 1.5(d)]. Switching between levels of abstraction becomes necessary in both understanding the details of the operation and optimizing the overall performance. In fact, in today's IC industry, the interaction among all groups, from device physicists to system designers, is essential to achieving high performance and low cost. In this book, we begin with device physics and develop increasingly more complex circuit topologies.

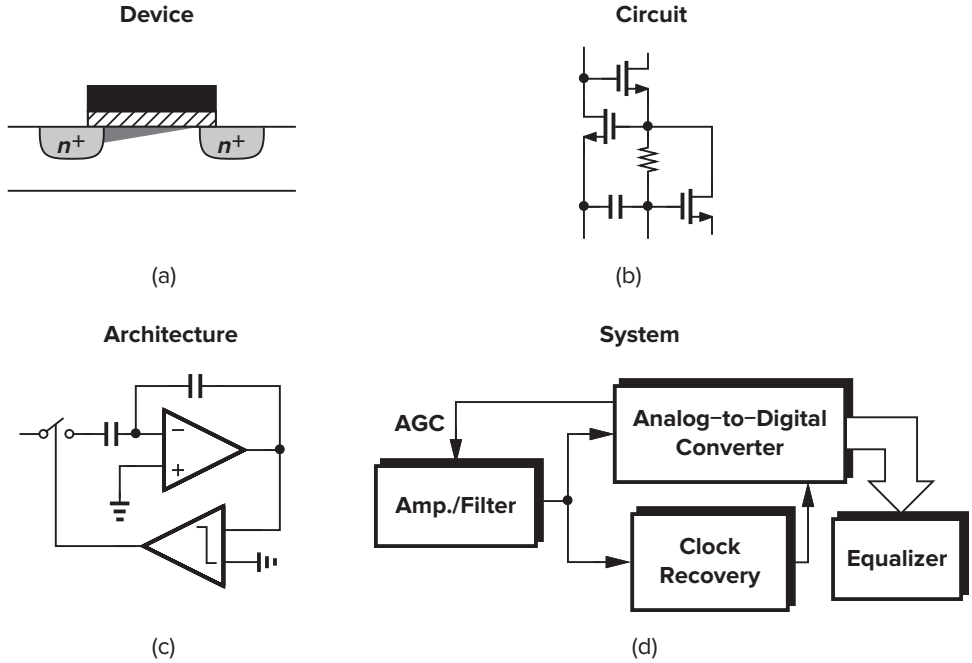


Figure 1.5 Abstraction levels in circuit design: (a) device level, (b) circuit level, (c) architecture level, (d) system level.

CHAPTER

2

Basic MOS Device Physics

In studying the design of integrated circuits (ICs), one of two extreme approaches can be taken, (1) begin with quantum mechanics and understand solid-state physics, semiconductor device physics, device modeling, and finally the design of circuits; or (2) treat each semiconductor device as a black box whose behavior is described in terms of its terminal voltages and currents and design circuits with little attention to the internal operation of the device. Experience shows that neither approach is optimum. In the first case, the reader cannot see the relevance of all the physics to designing circuits, and in the second, he or she is constantly mystified by the contents of the black box.

In today's IC industry, a solid understanding of semiconductor devices is essential—more so in analog design than in digital design, because in the former, transistors are not considered to be simple switches, and many of their second-order effects directly impact the performance. Furthermore, as each new generation of IC technologies scales the devices, these effects become more significant. Since the designer must often decide which effects can be neglected in a given circuit, insight into device operation proves invaluable.

In this chapter, we study the physics of MOSFETs at an elementary level, covering the bare minimum that is necessary for basic analog design. The ultimate goal is still to develop a circuit model for each device by formulating its operation, but this is accomplished through a good understanding of the underlying principles. After studying many analog circuits in Chapters 3 through 14 and gaining motivation for a deeper understanding of devices, we return to the subject in Chapter 17 and deal with other aspects of MOS operation.

We begin our study with the structure of MOS transistors and derive their I/V characteristics. Next, we describe second-order effects such as body effect, channel-length modulation, and subthreshold conduction. We then identify the parasitic capacitances of MOSFETs, derive a small-signal model, and present a simple SPICE model. We assume that the reader is familiar with such basic concepts as doping, mobility, and *pn* junctions.

2.1 ■ General Considerations

2.1.1 MOSFET as a Switch

Before delving into the actual operation of the MOSFET, we consider a simplistic model of the device so as to gain a feel for what the transistor is expected to be and which aspects of its behavior are important.

Shown in Fig. 2.1 is the symbol for an *n*-type MOSFET, revealing three terminals: gate (G), source (S), and drain (D). The latter two are interchangeable because the device is symmetric. When operating

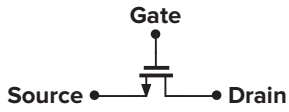


Figure 2.1 Simple view of a MOS device.

as a switch, the transistor "connects" the source and the drain together if the gate voltage, V_G, is "high" and isolates the source and the drain if V_G is "low."

Even with this simplified view, we must answer several questions. For what value of V_G does the device turn on? In other words, what is the "threshold" voltage? What is the resistance between S and D when the device is on (or off)? How does this resistance depend on the terminal voltages? Can we always model the path between S and D by a simple linear resistor? What limits the speed of the device?

While all of these questions arise at the circuit level, they can be answered only by analyzing the structure and physics of the transistor.

2.1.2 MOSFET Structure

Figure 2.2 shows a simplified structure of an n-type MOS (NMOS) device. Fabricated on a p-type substrate (also called the "bulk" or the "body"), the device consists of two heavily-doped n regions forming the source and drain terminals, a heavily-doped (conductive) piece of polysilicon[1] (simply called "poly") operating as the gate, and a thin layer of silicon dioxide (SiO_2) (simply called "oxide") insulating the gate from the substrate. The useful action of the device occurs in the substrate region under the gate oxide. Note that the structure is symmetric with respect to S and D.

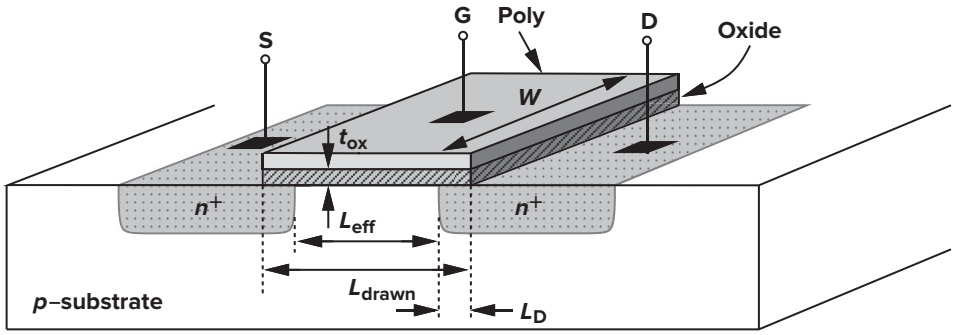


Figure 2.2 Structure of a MOS device.

The lateral dimension of the gate along the source-drain path is called the length, L, and that perpendicular to the length is called the width, W. Since the S/D junctions "side-diffuse" during fabrication, the actual distance between the source and the drain is slightly less than L. To avoid confusion, we write, $L_{eff} = L_{drawn} - 2L_D$, where L_{eff} is the "effective" length, L_{drawn} is the total length,[2] and L_D is the amount of side diffusion. As we will see later, L_{eff} and the gate oxide thickness, t_{ox}, play an important role in the performance of MOS circuits. Consequently, the principal thrust in MOS technology development is to reduce both of these dimensions from one generation to the next without degrading other parameters of the device. Typical values at the time of this writing are $L_{eff} \approx 10$ nm and $t_{ox} \approx 15$ Å. In the remainder of this book, we denote the effective length by L unless otherwise stated.

[1] Polysilicon is silicon in amorphous (non crystal) form. As explained in Chapter 18, when the gate silicon is grown on top of the oxide, it cannot form a crystal. The gate was originally made of metal [hence the term "metal-oxide-semiconductor" (MOS)] and is returning to metal in recent generations.

[2] The subscript "drawn" is used because this is the dimension that we draw in the layout of the transistor (Sec. 2.4.1).

If the MOS structure is symmetric, why do we call one n region the source and the other the drain? This becomes clear if the source is defined as the terminal that provides the charge carriers (electrons in the case of NMOS devices) and the drain as the terminal that collects them. Thus, as the voltages at the three terminals of the device vary, the source and the drain may exchange roles. These concepts are practiced in the problems at the end of the chapter.

We have thus far ignored the substrate on which the device is fabricated. In reality, the substrate potential greatly influences the device characteristics. That is, the MOSFET is a *four*-terminal device. Since in typical MOS operation, the S/D junction diodes must be reverse-biased, we assume that the substrate of NMOS transistors is connected to the most negative supply in the system. For example, if a circuit operates between zero and 1.2 volts, $V_{sub,NMOS} = 0$. The actual connection is usually provided through an ohmic p^+ region, as depicted in the side view of the device in Fig. 2.3.

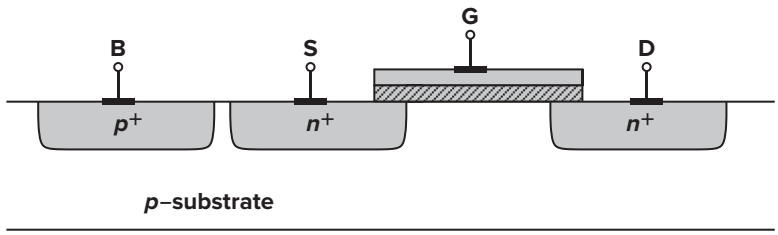


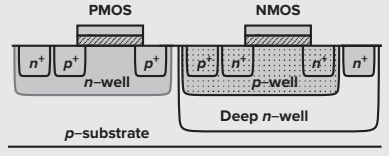
Figure 2.3 Substrate connection.

In complementary MOS (CMOS) technologies, both NMOS and PMOS transistors are available. From a simplistic viewpoint, the PMOS device is obtained by negating all of the doping types (including the substrate) [Fig. 2.4(a)], but in practice, NMOS and PMOS devices must be fabricated on the same wafer, i.e., the same substrate. For this reason, one device type can be placed in a "local substrate," usually called a "well." In today's CMOS processes, the PMOS device is fabricated in an n-well [Fig. 2.4(b)]. Note that the n-well must be connected to a potential such that the S/D junction diodes of the PMOS transistor remain reverse-biased under all conditions. In most circuits, the n-well is tied to the most positive supply voltage. For the sake of brevity, we sometimes call NMOS and PMOS devices "NFETs" and "PFETs," respectively.

Figure 2.4(b) indicates an interesting difference between NMOS and PMOS transistors: while all NFETs share the same substrate, each PFET can have an independent n-well. This flexibility of PFETs is exploited in some analog circuits.

Nanometer Design Notes

Some modern CMOS processes offer a "deep n-well," an n-well that contains an NMOS device and its p-type bulk. As shown below, the NMOS transistor's bulk is now localized and need not be tied to that of other NMOS devices. But the design incurs substantial area overhead because the deep n-well must extend beyond the p-well by a certain amount and must maintain a certain distance to the regular n-well.



2.1.3 MOS Symbols

The circuit symbols used to represent NMOS and PMOS transistors are shown in Fig. 2.5. The symbols in Fig. 2.5(a) contain all four terminals, with the substrate denoted by "B" (bulk) rather than "S" to avoid confusion with the source. The source of the PMOS device is positioned on top as a visual aid because it has a higher potential than its gate. Since in most circuits the bulk terminals of NMOS and PMOS devices are tied to ground and V_{DD}, respectively, we usually omit these connections in drawing [Fig. 2.5(b)]. In digital circuits, it is customary to use the "switch" symbols depicted in Fig. 2.5(c) for the two types, but we prefer those in Fig. 2.5(b) because the visual distinction between S and D proves helpful in understanding the operation of circuits.